6. TECHNICAL DESCRIPTION

6.1 CONTROL UNIT

The Control Unit contains two printed circuit boards, Control Board [600] and Audio Processing [601] and a membrane keyboard. In addition an optional Squelch Board [602] and an optional Line Transformer Board [603] may be installed. The Block Diagram of the Control Unit illustrates the functions of each circuit board while the Interconnection Diagram shows the interconnections between the boards.

6.1.1 CONTROL BOARD [600]

The primary functions of this module are to support the man/machine interface via keyboard and displays, control AUDIO PROCESSING [601] and communicate with TRANSCEIVER CONTROL BOARD [624] as a master by transmitting commands and receiving acknowledge and status messages in ASCII code according to a fixed protocol. This is accomplished through an embedded computer consisting of a microprocessor ("MPU") with the following on-chip facilities: 8 bits CPU, 128 bytes RAM used as buffer area and for saving internal variables, 2 ports of which one handles the transfer of a 16 bits packet to [601] controlling loudspeaker volume, selection of keying and audio signals using the signals (COMDATA), (COMCLOCK) and (COMLOAD), while the other is connected to a serial, asynchronous interface used for communicating at 300 baud via "RS 232C INTERFACE" with [624] using the signals (TUDATA) and (CUDATA), and finally a 16 bits timer used for generating 64 Hz real-time interrupts to switch the microprocessor from back- to foreground processing simultaneously measuring the period of the telemetry signals received from [624] representing signal strength and output power (i.e. (RXRATE) and (TXRATE) respectively) through "RATE MULTIPLEXER". The processor is clocked by a signal coming from "4 MHz XTAL OSCILLATOR" and is initialized by "MASTER CLEAR" combined with "MODE SWITCH". Due to "ADDRESS LATCH" being connected to the mutiplexed 8 bits wide data/address bus a full 16 bits wide address bus is available for the "MAP DECODER" to select between the connected memories and peripherals, which are the following: "PROGRAM ROM" (up to 12 kbytes of object code in EPROM), "CONFIGURATION PROM" (up to 4 kbytes in EPROM containing a list of up to 960 permitted TX frequencies and status code for enabled options of the equipment), "NON-VOLATILE RAM" (1 knibbles used for saving up to 76 RX/TX frequency pairs with corresponding modes and the present status of the equipment) powered by a lithium battery during power-off condition together with "REAL TIME CLOCK" which controlled by a 32.768 kHz crystal implements the watch function. By programming the latter it is possible to switch on the entire equipment automatically using the "OPTO COUPLER" to generate the galvanically isolated signal PWRON, which activates SMPS CONTROL [622].

Another peripheral circuit is the "KEYBOARD DISPLAY CONTROLLER", which constantly scans the membrane keyboard (organized as an 8x8 matrix) through "KEY SCAN DECODER" using the signals (DRV0--7) and (SEN0--7), while it simultaneously refreshes the entire display at a rate of 588 Hz (duty cycle 1/16) by utilizing "LED DECODER/LED DRIVER" and "DISPLAY DIGIT DECODER/DISPLAY DIGIT DRIVER" for multiplexing the annunciators and seven-segment displays respectively. The segments are driven from "DISPLAY SEGMENT DRIVER" and "DISPLAY SEGMENT DECODER" (performing the conversion from BCD-code). The displays may be dimmed through the last peripheral, "BEEP DIM REGISTER", by pulse width modulation via "PWM COUNTER". "BEEP DIM REGISTER" is also capable of controlling "PROGRAMMABLE DIVIDER" generating the signal SINCLOCK used by [601] to synthesize sinusoidal signals for modulation purposes and "beeping" (acoustic feedback to the operator signalling a key closure). In order to permit remote control, another "RS 232C INTERFACE" is available connected to a serial, asynchronous interface implemented by "ACIA". Both serial interfaces are clocked by "BAUD RATE DIVIDER", which is fed by a 1 MHz clock from "MPU".

6.1.2 AUDIO PROCESSING [601]

All power supply regulation in the Control Unit is performed on this board. Voltages of +24V, -15V, +15V, -15V are supplied from the Transceiver Unit. The +15V and one -15V line are current limited to approximately 0.7A before supplying the audio power amplifier in order not to disturb the function of the equipment in case of irregularities on the loudspeaker lines. For the same reason the current from the loudspeaker is returned in these -15V wires and not via the "GND" wire. All other circuits are supplied from the +24V and the second -15V voltage. To obtain the necessary regulation and isolation between the circuits, these voltages are stabilized in several small 0.1A regulators, supplying +/-12V and +6V for receiver AF-circuits, +/-12V and +6V for transmitter AF-circuits and +/-12V for the digital circuits. +5V to the Control Board [600] is derived from +24V by means of a switching regulator, capable of delivering 2A.

All functions on [601] are controlled by the microprocessor on [600] through a 3 wire serial interface. The 5V microprocessor-signals are level-shifted to the 12V logical level used on [601] and converted to a 16-bit parallel code. 3 bits control the key selector and the input selector. Before the signals enter the selectors, they pass through the filters, where they are filtered, limited and shaped (keysignals only). The microphone signal further passes through the microphone amplifier where the gain can be set from 0 to 15 dB by means of a potentiometer. A delay circuit makes it possible to delay the positive edge of the telex key signal from 0 to 30 ms in steps of 3.33 ms. The negative edge remains unaffected. Accuracy of the delaytime will be within one period of the reference clock signal from the microprocessor (0.42 ms). The selectors are controlled as follows:

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Mode	Keyselector	Inputselector
AM/R3E USB/LSB	Handset/aux.	Mic./aux.
CW	Morse	off
MCW	Morse	Sinetone
TELEX	Telex	Telex
ALARM SEND	Constant keyed	Sinetone
ALARM TEST	off	Sinetone

In the AM/SSB modes a keying signal from the handset will open the microphone input, and a signal from the aux. key input will open the aux. input. If both keying inputs are activated, the analog signals will be mixed.

The sinetone to the input selector is derived from a clocksignal produced by the microprocessor on [600]. The squarewave is converted in the square-to-sine converter circuit to a sinewave with a frequency 16 times lower than the clock-frequency. The sinetone frequency is 800 Hz in MCW mode and 1300 Hz/2200 Hz in the alarm-modes.

From the input selector the signal is led to the compressor circuit, where it is levelled to a 0 dBm (0.775V RMS) balanced signal before transmission to the Transceiver Unit. A checkdetector circuit informs the control board [600] when the inputsignal is compressed (in the -3 dBm -0 dBm range).

From the key selector the signal is led to the de-bounce circuit, which will cancel any bounce on the edges of the keying signal within approximately 10 ms from first level-shift. The signal is separated from the keyline to the Transceiver Unit by a class B driver stage. The signal is also transmitted to the control board [600]. The keyline also carries a frequency modulated signal from the Transceiver Unit to the Control Unit with information about the transmitter RF output power. The RX-RATE line carries a similar signal representing signal strength. These signals are amplified in two equal amplifiers before they continue to the control board [600].

The RX signal path on [601] starts with a check-detector, which registrates if the balanced lines from the Transceiver Unit carries a signal greater than approx. 0.5V RMS (nominal line level is 0.775V RMS). The input amplifier converts the differential signal to a single signal of the same level before it is fed to the Squelch Board [602] if provided. When it returns from [602] (or from a bypass plug in the socket) it enters the AF-switch. Here it is possible to select either the RX signal or the sidetone from the shaping circuit.

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Both shaping and AF-switch is controlled by the AF-output selector which combines RX/TX mode and keyline to obtain correct switch-timing (e.g. a 45 ms break-in time in CW and MCW modes). The clock reference is the same as for the telex key delay circuit.

From the AF-switch the signal enters volume control and line amplifier. The line output signal can be adjusted from 0 to approx. 2.4V RMS (+10 dBm) by means of a potentiometer. The volume control is build around an 8-bit digital-to-analog converter followed by a 20 dB attenuator in order to control the audio volume by the control board processor. The RX signal path further consists of a preamplifier, which also drives the earpiece, a speaker on/off switch and the audio power amplifier. The signal to the loudspeaker is monitored by a check-detector.

6.1.3 SQUELCH BOARD [602]

The Squelch Circuit is operating exclusively on the received AF-signal knowing its spectral distribution with and without the presence of speech. The AF-signal is fed to the AF-switch, which carries out the squelch function by turning on and off the AF-signal.

The AF-signal is also fed to the input of the High Pass Filter which prevents hum and low frequency noise from disturbing the Detector. The high pass filter output signal is converted into a squarewave by the Schmitt Trigger, and the resulting signal is led to the input of the Detector.

The Clock Generator produces a reference frequency for both Detector and Hold Circuit.

In the presence of speech the mean frequency of the AF-signal is lowered and becomes smaller than the detector frequency limit set by the reference frequency and the A-selector. This causes the Detector via the Hold Circuit to turn on the AF signal.

When speech ceases the AF-signal consists of noise only which increases the mean frequency above the detector frequency limit. The detector now triggers the Hold Circuit, which turns off the AF-signal after a certain hold time, set by the reference frequency and the B-selector.

6.2 TRANSCEIVER UNIT

The Rx/Tx Assembly of the Transceiver Unit contains the Rx/Ex Signal Path [610] a Synthesizer Board [611] and a Master Oscillator [612] (or [613], [614]). These boards are located in the door of the unit. The cabinet itself contains a Switched Mode Power Supply which converts the battery voltage to a stabilized 48V voltage supplying the Power Amplifier and the Voltage Converter Board [621]. The Voltage Converter produces various supply voltages necessary in the equipment and provides galvanic isolation from the battery. Supply voltages, signal- and control voltages are distributed via the Interconnection Board [620] to external units and to the Transceiver Control Board [624] which performs the central control of the Transceiver Unit.

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The exciter output signal from the Rx/Tx Assembly is routed to the Power Amplifier Board [626] the output from which is filtered by the harmonic filters on P.A. Filters [627] (or [628], [629]).

6.2.1 RX/EX SIGNAL PATH [610]

In the Rx/Ex Signal Path several of the components are common to both the Receiver and the Exciter. This applies to the SSB crystalfilter, the 45 MHz crystalfilter and the two passive mixers. Therefore several diodeswitches route the receiver signal and the exciter signal through the signal path.

6.2.1.1 Receiver

The antenna RF-signal is led through coax connector SK 1 to the protection circuit, which protects the receiver against excessive RF-voltages and static electricity discharges, appearing on the antenna.

Through the switchable antenna attenuator the RF-signal is led to the preselector consisting of six fixed-tuned band-pass filters and seven fixed-tuned notch filters. The band-pass filters cover the frequency bands 10-405 kHz, 405-527 kHz, 527-1600 kHz, 1600 kHZ - 4 MHz, 4-13.4 MHz and 13.4-30 MHz, respectively. The seven notch filters have the following notch frequencies: 6.1 MHz, 7.2 MHz, 9.65 MHz, 11.8 MHz, 15.3 MHz, 17.8 MHz and 21.6 MHz, respectively.

A change in receiver frequency will be followed by automatic selection from among the band-pass filters and the notch filters. The automatic selection is controlled from the Transceiver Control Board [624] via the serial data bus.

The RF-signal goes via the switchable RF amplifier to the double-balanced Schottky-diodes mixer,where it is mixed with the 45-75 MHz synthesizer signal from the Synthesizer Board [611] to generate the first intermediate frequency signal of 45 MHz.

The 45 MHz IF-signal is amplified in the grounded gate JFET amplifier and then filtered in the 45 MHz double sideband crystal filter, determining the overall AM selectivity.

Before being fed to the 2nd mixer, the IF-signal is passing through the MOSFET amplifier which has a variable gain controlled by the delayed AGC voltage.

The 2nd mixer converts the 45 MHz IF signal to the 1.4 MHz IF signal by mixing with a 43.6 MHz synthesizer signal from the Synthesizer Board [611].

After amplification in the grounded gate JFET amplifier, the 1.4 MHz signal is fed to the Information filter bank.

Depending on the version (i.e. crystal filter options) and the selected mode, the 1.4 MHz signal is routed through one of the filters X2, X3, X4, X5 or the wide filter, controlled by the Transceiver Board [624] via the serial data bus.

The now filtered 1.4 MHz signal is amplified in the 1.4 MHz amplifier strip IC6, Q19 and Q21. The voltage gain of the amplifier strip is controlled partly by the AGC voltage applied to IC6 and partly by the control line "IF-GAIN", which, when in logical high condition, increases the gain of Q19 with approx. 12 dB.

Q20 shortcircuits the signal path, when receiver muting takes place.

From the IF-strip, the signal is fed to the Signal Detector IC5.

The integrated circuit of the Signal Detector contains a balanced mixer and a high-gain limiting amplifier. The IF-signal is applied to the one input port of the mixer.

In the modes H3E and H2A, the IF-signal is also fed to the amplified input. This signal is amplified and clipped to constant amplitude and internally connected to the other input port of the mixer where it is mixed with the modulated signal. The difference frequency contains the wanted AF signal.

In other modes but H3E and H2A a 1.4 MHz signal, derived from the Synthesizer Board [611], is applied to the amplifier input.

The unbalanced AF-signal is filtered and converted to a balanced signal before it is fed to the flat-cable connector PL1.

From the IF-strip the signal is also fed to the AGC Detector consisting of two transistors in the integrated array IC8. The signal, which is now rectified to a dc-voltage, is applied to the AGC Timing Circuit. The AGC voltage from the AGC Timing Ciurcuit controls the overall gain of the receiver. The AGC voltage is also fed to the Transceiver Control Board [624], where it is used in self-check routines and, by means of a voltage to frequency converter, fed to the Control Unit controlling the signal strenght meter on the front panel.

When manual gain control (MGC) is selected the Transceiver Control Board [624] generates a dc voltage which is fed to the receiver signal path instead of the AGC voltage.

6.2.1.2 Exciter

The balanced AF-signal with a level of 0 dBm/600 ohm, is applied to the double balanced mixer IC9, where it is mixed with a 1.4 MHz signal from the Synthesizer Board 611 and applied to the mixer through the limiting amplifier in the integrated circuit IC5.

A check signal is derived from the AF input and is used in the self-check routines.

The double sideband suppressed carrier from the mixer is filtered by the lower sideband crystal filter connected to the output of the mixer and applied to the 1.4 MHz sideband amplifier.

In the 1.4 MHz amplifier the lower sideband signal from the crystalfilter is combined with a 1.4 MHz carrier signal from the Synthesizer Board [611].

The level of the lower sideband signal and that of the 1.4 MHz carrier signal are regulated in the attenuators according to the selected operation mode before the combination, controlled from the Transceiver Control Board [624] via the serial bus.

The peak to peak voltage of the combined signal appearing at the output of the 1.4 MHz amplifier is independent of the operation modes.

The combined 1.4 MHz signal is mixed with a 43.6 MHz signal from the Synthesizer Board [611] in a passive double balanced mixer to form an IF-signal of 45 MHz.

The 45 MHz IF-signal is amplified in a grounded gate JFET amplifier, filtered in the 45 MHz crystal filter, and then fed to the ALC attenuator.

The ALC attenuator form the regulation circuit in the ALC system of the Transceiver. The attenuation is controlled by a dc voltage from the Transceiver Control Board [624].

In the passive double-balanced mixer, the 45 MHz IF-signal is finally mixed with a high-sided (45-75 MHz) local oscillator signal from the Synthesizer Board [611] converting the 45 MHz signal to a RF-signal at the actual transmitting frequency.

The RF-signal is fed to the exciter output amplifier through a low-pass filter. The RF-signal detector placed at the output of the amplifier, is used in the self-check routines.

6.2.1.3 Interface circuit (Sub diagram 5)

Parallel to serial out.
The version information is transmitted to the Transceiver Control Board [624] via the serial data bus Stat Data. The actual version is indicated by means of version jumpers 1 to 9 and by means of an automatically grounding of IC13 terminals 3, 14, 13 and 12 when crystal filters are mounted in position X5, X4, X3 and X2, respectively. When Stat Load changes to low condition the version information is loaded into the parallel-load 8-bit shift registers IC12 and IC13. Serial data transfer occurs on the positive edge of the clock.

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Serial to parallel in.
Most of the control data from the Transceiver Control Board [624] are transmitted to the Rx/Ex Signal Path via the serial data bus, Com Data. In the 8-stage shift-and-store Bus registers IC14 to IC17 data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register and appears at the output, when Com Load changes to high.

The fast control signals $\overline{Tx}/Rx$, $\overline{Rx\ Mute}$ and shape key are applied to the board in parallel.

$\overline{Tx}/Rx$ controls the supply voltages to the separated Rx and Ex circuits. When in high condition supply voltages are applied to the Exciter circuits. When in low condition, supply voltages are applied to the Receiver circuits.

The receiver signal path is muted, when $\overline{Rx\ Mute}$ is in low condition, independent of other control signals.

The Shape Key controls the exciter signal shaping via the Ex key switch (sub diagram 3).

6.2.2 SYNTHESIZER BOARD [611]

6.2.2.1 45-75 MHz Synthesizer

The 45-75 MHz Synthesizer is of the Fractional-N type and has a frequency resolution of 10 Hz.

The 40.96 kHz reference frequency derived from the Master Oscillator [612] is fed to both Phase Comparator and Phase/Frequency Comparator. Likewise the output signal of the Loop Divider is fed to both comparators.

When the loop is locked the Phase/Frequency Comparator is turned off and there exists no difference in frequency, but a definite and time varying phase difference between the reference signal and the Loop Divider output signal. The Phase Comparator compares the phase of the two signals and if it differs from the steady state value, the Phase Comparator will produce a correction signal, which via the Loop Filter corrects the frequency and phase of the VCO until the steady state phase difference is reestablished.

If the phase difference exeeds the limits of the Phase Comparator, for example during change of the synthesizer output frequency, the Phase/Frequency Comparator is automatically turned on. It will override the Phase Comparator by producing a correction signal which via the Loop Filter will alter the frequency and phase of the VCO until the difference between the reference signal and the Loop Divider output signal is well inside the working limits of the Phase Comparator. After a short amount of time the Phase/Frequency Comparator is turned off and the Phase Comparator takes over again ending up with the steady state locked condition.

The Loop Filter is capable of changing parameters when required by means of four diodes. When the loop is locked the diodes are turned off, and in this condition the Loop Filter is designed to prevent noise modulation of the VCO and to give the loop a good dynamic response. During a major change in the synthesizer output frequency the diodes are turned on, and in this case the Loop Filter is designed to give the loop a fast dynamic response.

The VCO covers a frequency range of 45-75 MHz which is divided in 4 bands. The bands are selected by the microprocessor on the Transceiver Control Board 624. The amplitude stabilized output signal of the VCO is split between two buffer amplifiers. One for the output signal of the synthesizer, which is led to the 1st mixer on the Rx/Ex Signal Path 610, the other buffer amplifier drives the input of the Loop Divider.

The Transceiver Control Board determines the output frequency of the synthesizer by loading the corresponding division ratio into the Loop Divider and the Binary Accumulator. The integer part of the division ratio is stored in the Loop Divider and the fractional part is fed to the one input of the Binary Accumulator.

The 12-bit Binary Accumulator enables 10 Hz resolution of the synthesizer output frequency. The output of the Binary Accumulator is fed back to one of it's own inputs and in that way added to the fractional division ratio fed to the other input. The sum is transferred to the output of the Binary Accumulator when it receives an Accumulator Clock Signal. This happens in every period of the loop divider output frequency. When the sum exeeds the maximum capacity (4095) of the Binary Accumulator, it produces an Accumulator Carry Signal, and the remainder of the contents is kept for the next addition. The carry signal increases the division ratio of the Loop Divider by one. The loop will respond to this increase by producing an output frequency corresponding to the fractional division ratio.

The time varying phase difference between the reference signal and the loop divider output signal, caused by the said increase in the division ratio, is a function of the fractional division ratio. This function is derived from the output of the Binary Accumulator and converted into a current by the DA-Converter. The current is fed to the Phase Comparator where it cancels the signal produced by the time varying phase difference and thus preventing modulation of the VCO.

The frequency information, loaded by the microprocessor on the Transceiver Control Board 624, is fed to the Ramp Current Generator, resulting in a current directly proportional to the output frequency of the synthesizer. As the Ramp Current controls the gain of the Phase Comparator, the dynamic response of the loop is held constant over the entire frequency range of the synthesizer.

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If the said cancellation of the time varying phase difference isn't complete, the Ramp Current Correction circuit measures the error at the Phase Comparator output and automatically adjusts the Ramp Current Generator until cancellation is obtained.

Two signals derived from the Phase Comparator and the Phase/Frequency Comparator are combined in a check circuit with the check signals from the 43.6 MHz and 1.4 MHz Synthesizer resulting in a final check signal led to the Transceiver Control Board.

6.2.2.2 43.6 MHz Synthesizer

The synthesizer used is of the fractional-N type, which refers to the fact that the smallest step in output frequency is not equal to the reference frequency but a fractional part of this.

From the Master Oscillator 612 a 1.28 MHz signal is led to the Reference Divider which divides the signal by 10 having a 128 kHz reference frequency at the input of the Phase/Frequency Comparator.

The 128 kHz reference frequency and the output frequency of the Loop Divider are compared in the Phase/Frequency Comparator. When the loop is locked there exists no difference in frequency but a definite and time varying phase difference between the two signals. If the loop is out of lock the Phase/Frequency Comparator will produce a correction voltage which will alter the frequency and phase of the VCXO until the loop is back in the locked condition.

The Loop Filter is designed to give the loop a good dynamic response and to stop noise modulation of the VCXO.

The VCXO covers a frequency range of 14.53333 MHz +1.333 kHz/-1 kHz. The output signal of the VCXO is fed to the Tripler where the frequency is mutiplied by 3, resulting in a synthesizer frequency of 43.6 MHz + 4 kHz - 3 kHz.

The signal from the Tripler is amplified in the Buffer Amplifier and the level-stabilized output signal is led to the 2nd Mixer on the Rx/Ex Signal Path 610. Another signal derived from the Buffer Amplifier is fed to the input of the Loop Divider.

A 7-bit Binary Accumulator is incorporated in order to obtain a fractional division ratio in the loop, giving a 1 kHz step capability of the synthesizer output frequency. By loading the fractional division ratio into the input of the Binary Accumulator, the microprocessor on Transceiver Control Board determines the output frequency of the synthesizer. The other input of the Binary Accumulator is connected to its output. The two inputs are added and the sum is transferred to the output when the Binary Accumulator is clocked. The clock input is connected to the output of the Loop Divider.

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When the sum exeeds the maximum capacity (127) of the Binary Accumulator it produces an Accumulator Carry Signal which increases the ratio of the Loop Divider by one, and the remainder of the accumulator contents is kept for the next addition. The loop responds to this increase by producing an output frequency corresponding to the fractional division ratio.

As a result of the variation in the division ratio, the phase difference between the reference frequency and the output frequency of the Loop Divider will be varying and a function of the fractional division ratio.

This function is derived from the output of the Binary Accumulator and converted into a voltage by the DA-converter. The output signal of the Phase/Frequency Comparator caused by time varying phase difference is cancelled at the input of the Loop Filter by the output voltage of the DA-converter, and thus preventing modulation of the VCXO.

The 128 kHz reference frequency and a signal derived from Phase/Frequency Comparator are combined in the Check Detector to give information of the synthesizer lock status.

6.2.2.3 1.4 MHz Synthesizer

The synthesizer consists of a Loop Filter, a 5.6 MHz VCO, a Buffer Amplifier and a single integrated circuit which contains both Reference Divider, Loop Divider and Phase/Frequency Comparator. The division ratio of the Reference Divider and the Loop Divider are controlled by the microprocessor on the Transceiver Control Board [624].

A 1.28 MHz signal from the Master Oscillator [612] is fed to the input of the Reference Divider and divided by 3200, thus obtaining a reference frequency of 400 Hz as well as a frequency step size of 400 Hz for the synthesizer loop.

The reference frequency and the Loop Divider output frequency are compared in the Phase/Frequency Comparator. In the locked condition there exists no difference between the two signals neither in frequency nor in phase. If a difference occurs, say during a change of the synthesizer output frequency, the Phase/Frequency Comparator will produce a correction voltage which will correct the frequency and phase of the VCO until the locked condition is obtained again.

The Loop Filter is designed to give the loop a proper dynamic response and to prevent noise from modulating the VCO.

The 5.6 MHz VCO covers the frequency range from 5.582 MHz to 5.612 MHz. The output signal of the VCO is amplified in the Buffer Amplifier and then split into two, one for the input of the Loop Divider and one for the Divide-by-4 circuit.

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The output frequency range of the Divide-by-4 circuit is 1.4 MHz + 3 kHz/4.5 kHz and the frequency step size is 100 Hz.

The output signal of the Divide-by-4 circuit is fed to the Output Filter where the harmonics of the signal are reduced and the exact output level is set. The output signal is led to the 3rd Mixer on the Rx/Ex Signal Path [610] .

A check detector is incorporated to indicate the lock status of the synthesizer.

6.2.3 MASTER OSCILLATOR [612] [613] [614]

The three Master Oscillators available all consist of the same circuits but have different frequency stabilities determined by the 10.24 MHz Temperature Compensated Crystal Oscillator (TCXO) used.

The output signal of the TCXO is split between two reference dividers. One for the 45-75 MHz Synthesizer and one for the 43.6 and 1.4 MHz Synthesizers.

The Reference Divider, 45-75 MHz Synthesizer, divides the 10.24 MHz TCXO signal by 250 having a 40.96 kHz reference frequency at two outputs.

The Reference Divider, 43.6 and 1.4 MHz Synthesizer, divides the 10.24 MHz TCXO signal by 8, obtaining a 1.28 MHz signal fed to two outputs.

The output signals of the divider are fed to the Check Detector to detect the presence of both. The resulting check signal MO-Check is via the Synthesizer Board [611] fed to the Transceiver Control Board [624] .

For Master Oscillator [613] a heater (TCXO Heater [699]) is incorporated in order to keep the TCXO ambient temperature above 0 deg. Celcius.

6.2.4 SWITCHED MODE POWER SUPPLY

The DC-power, deriving from the battery, first has to pass an input filter and then a relay switch controlled by the overvoltage and reverse polarity protection circuit, before it is allowed to flow to the converter circuit. The converter is a boost-converter combined with a push-pull converter allowing the converter to handle duty cycles higher than fifty percent. The converter does not provide galvanic isolation. The regulating loop has been designed in order to keep the output voltage from the converter fairly stable independent of battery voltage variations and different loading conditions on the put. This is done by regulating the duty cycles of the pulses, deriving from a 25 kHz oscillator, IC6 before they are forming the driving signal for the converter driver.

The duty cycle regulation is located on board [622] and consists of IC1, IC2, IC6, Q3 and Q4. D12 ensures that the duty cycle does not rise to more than ninety percent.

The total current in the converter is measured by means of T2, T3 and is used for the current limiting circuit located on board 622. The output is also equipped with an overvoltage protection circuit Q9 and Q25 on board 622.

The mains relay switch is activated by a bistable circuit Q1, Q2, RL1 and is protected from "Welding" by IC3. IC4 prevents the main relay from being closed when the input voltage rises to more than 42 volts. These components are located on board 622.

6.2.5 VOLTAGE CONVERTER BOARD 621

The voltage converter is a push-pull converter with isolation. There is no stabilisation, it only converts the stabilized 48 V voltage from the Switched Mode Power Supply. The converter frequency is controlled by IC2 and IC5. The converter starts when the enable input is high. The output is protected by a Short Circuit Sequencer. During a shortcircuit the gate voltage of Q10 and Q11 is controlled by Q5 so that the current through Q10 and Q11 is limited to approx. 3 A and sensed by R20.

A sequence network, consisting of IC1, IC2, IC3 and IC4 is sensing the gate voltage of Q10 and Q11. If the voltage is low, the converter is shut-off for 308 msec. and then restarted as the shortcircuit sequencer is disabled for 10 msec. by IC4, thus allowing the converter to work for 10 msec. charging the output capacitors. In case of no shortcircuit the gate voltage of Q10 and Q11 will be high and the converter will continue to work. In case of a shortcircuit the gate voltage of Q10 and Q11 will remain low and the sequence network shut off the converter for 308 msec. etc. This means that the loss in Q10 and Q11 will be reduced by a duty factor 1:30. At the same time the current in the output circuit will be reduced and the wiring thereby protected.

6.2.6 TRANSCEIVER CONTROL BOARD 624

This module implements the following functions: Communication with CONTROL BOARD 600 as a slave by receiving and executing command messages in order to control RX/EX SIGNAL PATH 610, SYNTHESIZER BOARD 611, PA FILTERS and ATU BOARD 640, and by transmitting acknowledge and status messages back to 600. To achieve this, a structure similar to that described in the section concerning 600 is used: The "MPU" communicates with its counterpart on 600 using (TUDATA) and (CUDATA) via "RS 232C INTERFACE". Status of 610 (i.e. crystal filters installed) is read as a 16 bits packet using the signals (STAT DATA RX/EX), (CLOCK) and (STAT LOAD), while commands are transferred from 624 in the form of a 32 bits packet using (COMDATA), (CLOCK) and (COM LOAD RX/EX). This processor is also clocked by a " 4 MHz XTAL OSCILLATOR " and is initialized by a "WATCHDOG" capable of automatically restarting a stalled program, which does not issue a 32 Hz trigger signal combined with "MODE SWITCH". "ADDRESS LATCH" and "MAP DECODER" operate in the same manner as on 600, "PROGRAM ROM" holds 8 kbytes in EPROM, while "SCAN BUFFER RAM" (1 knibbles) is used for holding the programmed scanning channels.

The frequency synthesizers on 611 are controlled via multiplexed data(SYNDATA 0--3) and address busses (SYNADR 0--2) using (SYNSTRO 0--5), whereas the corresponding switching between transceiving states on 610 is done by proper sequencing of the signals (TX/RX), (SHAPEKEY) and (MUTING) triggered by transitions of the signal (KEYLINE) originating from AUDIO PROCESSING 601 . (KEYLINE) is also modulated by "VF CONVERTER" to carry a telemetry signal representing output power back to 600 via 601 . Two analog loops are located on this board. The most simple is associated with the receiving state of 610 through "MGC REGISTER" and the corresponding DAC driving "MGC LOOP" connected to another "VF CONVERTER" generating a new telemetry signal representing received signal strength (RXRATE). The other loop ("PA STRESS MONITOR/ALC LOOP") stabilizes the output in the transmitting state by comparing the output of the "SETPOINT REGISTER" and the corresponding DAC with the signals FILPEAK, PAPEAK and IANTAVR in order to generate the error signal ALC used for driving an electronically controlled attenuator placed in the transmitter signal path. Finally, another signal controlled from the processor is generated using "ALC-HOLD REGISTER" and the corresponding DAC to make the gain of the transmitter signal path independent of the modulating signal. To increase the number of peripherals on this board beyond the capacity of "MAP DECODER" indirect addressing is introduced by using "SYNTHESIZER/MUXDATA REGISTER" not only for driving the synthesizers but also as a local bus feeding the following registers: "PA/LP REGISTER" (controls the relays switching the PA FILTERS depending on the TX frequency via "RELAY DRIVERS" and the power to POWER AMPLIFIER BOARD 626), "MULTIPLEXER REGISTER" (controls a 16-to-1 multiplexer "MUX" used for monitoring diagnostic and status signals) and "SETPOINT REGISTER" (allready mentioned). Directly driven from the databus are "STROBE REGISTER" (strobes the synthesizer as described earlier) and "SIGNAL PATH REGISTER", which via "BUFFERS" controls the keying signals mentioned before. The handshake protocol with the processor located on 640 uses the signals (TUNE) and (TPR). The status of 640 is constantly monitored via (SWROK) and (TCO) and any changes detected are signalled to 600 using appropriately coded messages. In the same way 626 is monitored via (TC1) and "PA STRESS MONITOR/ALC LOOP". The signals (FILTYP 0--3) and (750/250) from PA FILTERS and 640 are used for identifying purposes by the "MPU".

6.2.7 POWER AMPLIFIER 626

The Power Amplifier contains four active stages and has a total power gain of approx. 42 dB.

The RF signal from the Exciter passes through the input-attenuator, where the gain may be adjusted within a 3 dB range, and where the gain is reduced by 14 dB when "Low Power" is activated or if a fault should occur in the ALC-loop.

The signal is then amplified approx. 23 dB in the Class-A Driver stages 1 and 2 and approx. 12.5 dB in the Class-AB push-pull Driver stage 3, before being fed into the final Power Amplifier stage, which also works in Class-AB push-pull, with a gain of approx. 12.5 dB and the capability of delivering 250 W into a 50 ohm load.

The DC output from the peak-detector, which monitors the reflected power and output voltage, is connected to the ALC-circuit on the microprocessor-board and to the input-attenuator via the protection-circuit. The input-power is then reduced via the ALC-loop if the reflected power from the load exeeds approx. 25 W during mismatch conditions.

The Bias stabilizer circuits provide adjustable stabilized bias voltages from the 5 V source and supplies the bases of the Class-AB amplifier stages, so that the quiscent currents may be adjusted.

The key-circuits give a 24 V stabilized voltage from the 48 V source, which supplies Driver 1 and 2 and enables the bias circuits whenever "Key" is activated.

Thermoswitch SW2 will close and reduce the input power if the heatsink temperature exeeds 100 deg. C and thermoswitch SW1 will open and remove the supply voltage from Drivers 1, 2 and 3 if the heatsink temperature exeeds 110 deg. C.

6.2.8 P.A. FILTERS

6.2.8.1 P.A. FILTERS, Marine Bands [627]

The filterbank contains 6 lowpass-filters covering the maritime bands in the frequency range 1.6-27.5 MHz, as shown in the table below.

Filter no.	Passband MHz	Stopband MHz	Relays A	B	C
1	1.60- 2.31	3.19	0	1	0
2	2.31- 3.33	4.61	1	1	1
3	3.33- 4.80	6.64	1	0	0
5	6.20- 8.95	12.40	1	1	0
6	12.23-17.65	24.40	0	1	1
8	18.78-27.10	37.45	0	0	0

0 = off

1 = on

All filters are 5th order elliptic LP-filters (cauer-filters) with a series coil giving an inductive input inpedance on the harmonics. When loaded with 50 ohms the input SWR is less than 1:1.1 and the insertion loss less than 0.2 dB in the passbands. In the stopbands the attenuation is better than 25 dB.

The filters are inserted by a system of dual-pole dual-throw Relays controlled from the Transceiver Control Board [624] as shown in the table. Other types of filterbanks are available, and the microprocessor selects the corresponding switch pattern by sensing the type code information on 4 lines of the connector cable. If the cable is disconnected filter no. 8 is chosen, so that transmission is possible on all frequencies in case of fault in the switching system.

The DC voltage from the output peak-detector, which monitors voltage and current in the load, is connected to the ALC-circuit on the Transceiver Control Board [624]. This voltage is used for automatic adjustment of output power and should be 9.0 V for an output of 250 W into 50 ohms.

6.2.8.2 P.A. FILTERS, Continuous Coverage [629]

The filterbank contains 8 lowpass filters covering the frequency range 1.6-30.0 MHz, as shown in the table below.

Filter no.	Passband MHz	Stopband MHz	Relays A	B	C	D
1	1.60- 2.31	3.19	0	1	0	0
2	2.31- 3.33	4.61	1	1	1	0
3	3.33- 4.80	6.64	1	0	0	1
4	4.80- 6.93	9.58	1	0	0	0
5	6.93-10.00	13.85	1	1	0	0
6	10.00-14.42	19.95	0	1	1	0
7	14.42-20.80	28.80	0	0	0	1
8	20.80-30.00	41.00	0	0	0	0

0 = off
1 = on

All filters are 7th order elliptic LP-filters (cauer-filters) with a series coil giving an inductive input impedance on the harmonics. When loaded with 50 ohms the input SWR is less than 1:1.12 and the insertion loss less than 0.25 dB in the passbands. In the stopbands the attenuation is better than 47 dB.

The filters are inserted by a system of dual pole dual throw relays controlled from the Transceiver Control Board [624] as shown in the table. Type-code information is given via 4 lines of the connector cable. The function of the output peak detector is described in section 6.2.8.1.

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6.2.9 50 OHMS ANTENNA RELAY [630]

When the TRP 8250S is used without the Antenna Tuning Unit, a 50 ohms Antenna Relay- Board can be incorporated in the TRP 8250S. The Antenna Relay is a fast switching Simplex Relay (<5 msec) permitting ARQ-telex on one 50 ohms antenna. The Relay is controlled from [620] TS1 normally used to control the Antenna Tuning Unit.

6.3 ANTENNA TUNING UNIT

6.3.1 The ATU consists of a Tuning Network, a Measuring System and a Microprocessor Part. During the tune sequence a 6 dB Attenuator is switched in to keep the load of the Power Amplifier at approx. 50 ohms. The MPU will set up the Tuning Network to give the best obtainable SWR, on basis of the measuring system.

The Tuning Network comprises Capacitor Bank I, Capacitor Bank II and an Inductor Bank. With these it is possible to form either an L- or a pi- matching network. The capacitor Banks and the Inductor Bank are built up by binary related capacitors respectively binary related coils. The setting of the Capacitors and Coils is accomplished by relays.

In the measuring system a Directional Coupler extracts information about forward and reflected RF-voltages. A 0 deg. Phasecomparator detects the phase difference between line and forward voltages, and the result is fed to the MPU via an Amplifier. A 90 deg. Phase-comparator detects the phase difference between forward and reflected voltages and the output is fed to the MPU via an Amplifier. Two detectors rectify forward and reflected voltages, and feed them to the MPU to calculate the SWR. The MPU choses the setting of the tuning network, on basis of the detector inputs. The output ports from the MPU are lead to the Port Expansions and Relay Drivers to control the Relays.

The ATU is fitted with manual tuning switches for the 2182 kHz manual tune set-up (see section 7.9).

6.3.2 When a TUNE pulse is received from the Transceiver Unit the first steps are:

- to inhibit keying
- to insert the 6 dB attenuator
- to measure and store the reference voltages of the detectors
- to send a Tune Power Request to the Transceiver Unit.

The next steps are:

- to reset the tuning set-up, i.e. all capacitors disconnected and all coils shortcircuited and bypassed. The bypass relay is incorporated to lower the selfinduction
- to measure the antenna impedance.

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Measuring of the antenna impedance involves the two phase-detectors. On basis of the detector outputs the MPU will define the antenna impedance to be in one of four possible impedance areas. From the 90 deg. phase-detector the MPU determines if the impedance|Z| is less or greater than 50 ohms, and from the 0 deg. phase-detector the MPU determines if the antenna is either inductive or capacitive. The four possible impedance areas and corresponding detector input voltages to the MPU are listed below. The detector voltages refer to Vref which is for both detectors half the supply voltage, i.e. 2.5 V.

1. Inductive or purely resistive:	0 deg. detector	<= Vref
|Z| < 50 ohms:	90 deg. detector	> Vref
2. Capacitive:	0 deg. detector	> Vref
|Z| < 50 ohms:	90 deg. detector	> Vref
3. Capacitive:	0 deg. detector	> Vref
|Z| >= 50 ohms:	90 deg. detector	<= Vref
4. Inductive or purely resistive:	0 deg. detector	<= Vref
|Z| >= 50 ohms:	90 deg. detector	<= Vref

Having located the antenna impedance to be in Area 1 the tuning procedure is:

to increase the capacitance in Capacitor Bank I
until the impedance is purely resistive
(0 deg. detector ≃ Vref)
to measure the admittance.

The admittance Y is separated in two areas.

1. Y > 0.02 mho:	90 deg. detector > Vref
2. Y <= 0.02 mho:	90 deg. detector <= Vref

For Y > 0.02 mho: Tuning procedure A is used:

Capacitor Bank I is reset. By increasing the inductance in the Inductor Bank the impedance is transformed to lie as close as possible to Impedance Area 4 but with the impedance still being in Area 1. Then the capacitance in Capacitor Bank I is increased until Area 4 is reached, i.e. 90 deg. detector <= Vref, and then the inductance is decreased until Impedance Area 1 is reached again. This increasing of capacitance and decreasing of inductance continues until the output from the 0 deg. detector > Vref. The antenna impedance is then transformed within one bit of resolution to constitute a pure resistance of 50 ohms, seen from the Power Amplifier.

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The MPU finally calculates the SWR for the two nearest settings, choses the best, and the tuning is completed.

For Y <= 0.02 mho: Tuning Procedure B is used:

Capacitor Bank I is reset, and by means of Capacitor Bank II the impedance is transformed to Impedance Area 2, i.e. 0 deg. detector > Vref and 90 deg. detector > Vref.

To optimize the efficiency, the MPU calculates the reflection coefficient p (Vreflected divided by Vforward).

If rho < 0.66, the Tuning Procedure A is used to complete the tuning. The capacitance of Capacitor Bank II is retained.

If rho >= 0.66, the inductance of the Inductor Bank is increased until Impedance Area 3 is reached. Then the capacitance of Capacitor Bank II is decreased until Impedance Area 2 is reached again and so forth until rho < 0.66. Now the Inductor Bank will be reset and Tuning Procedure A will take over and finalize the tuning.

If the antenna impedance is located to be in Area 2, Tuning Procedure A is chosen.

If the antenna impedance is located to be in Area 3 the first steps are:

to increase the inductance of the Inductor Bank
until the impedance is purely resistive
(0 deg. detector ≃ Vref)
to measure the admittance Y
to reset the Inductor Bank.

For Y > 0.02 mho: Tuning Procedure A is used.

For Y <= 0.02 mho: Tuning Procedure B is used.

If the antenna impedance is located to be in Area 4, Tuning Procedure B is used.

When the tuning is completed, Tune Power Request is inhibited, the Tune Attenuator bypassed and the ATU is ready for transmitting.

6.3.3 There are a few circuits incorporated in the ATU, not directly related to the tuning procedure.

A current transformer at the antenna output terminal is used for measuring the antenna current. The transformed current is rectified, amplified and used as signal for the Antenna Current Display in the Control Unit.

To prevent overload of the relays a current sensing transformer is incorporated. The output from the current transformer is rectified and fed to an amplifier. The output from this is led to the ALC circuit in the Transceiver Unit to decrease the output power if the maximum permissible current is exceeded.

To prevent overheating of the Antenna Tuning Unit a temperature sensor is incorporated which at excessive temperatures commands the Transceiver Unit to reduce the output power by 5 dB.

The MPU constantly monitors the SWR at the input of the tuner and if it exceeds approximately 3 the Power Display Annunciator in the Control Unit starts to flash.

6.3.4 As an option an Antenna Relay Board [641] can be incorporated in the Antenna Tuning Unit.

The Antenna Relay is a fast switching Simplex relay permitting ARQ-telex on one antenna. It also contains a dummy-load and acts as grounding relay, connecting the antenna to ground when the equipment is switched off.

6.4 AC POWER SUPPLY UNIT

The P 8250 is a combined AC/DC Power Supply especially developed for powering the TRP 8250 Series. The input power for P 8250 is AC, and the output is an unregulated 32 V DC voltage.

Where a battery is required as a reserve source of electrical energy to the radiotelephone equipment, it can be connected via the P 8250 power supply. By means of the switch on the front panel it is possible to select between AC or Battery operation.

Primary connections of mains transformer

The primary connections of the mains transformer must be wired according to the diagram inside the cover of the unit depending on the mains voltage.

Fuse ratings

Only one fuse is used in the system, the Mains fuse FS 1 on the front panel.

From the factory the P 8250 is normally delivered wired for 220 VAC, and therefore the fuse mounted is a 6A3 slow type.

The fuse ratings are as follows:

Mains voltage (volt)	Fuse FS 1 (size 6.3 X 32 mm)
110/120	12A5 (slow)
220/240	6A3 (slow)

6.5 ALC AND PROTECTION SYSTEM

6.5.1 Automatic Level Control (ALC)

The TRANSCEIVER UNIT has an advanced microprocessor controlled automatic level system, which ensures that the optimum power is delivered to the ANTENNA TUNING UNIT.

The Tune Sequence, which is initiated either by pressing TUNE on the CONTROL UNIT front panel or by keying the transmitter after a frequency change has been carried out, is terminated by a CW pulse of full power with a duration of 70 ms.

The signal level at the output of the TRANSCEIVER UNIT is measured by means of a voltage and current peak-detector placed at the output of the P.A. FILTER ASSEMBLY 627 628 or 629 . The detector voltage (9.0 V at 250 W output power) is applied to the TRANSCEIVER CONTROL BOARD 624 , PL3-9 (FILPEAK), and compared with the output voltage (8.62 V) of the "SETPOINT REGISTER" in IC42-3,2. The error signal ALC is fed to the RX/EX SIGNAL PATH 610 , PL1-12 driving a voltage controlled attenuator placed in the exciter signal path.

Finally the ALC viltage is compared in IC42-5,6 with a ramp voltage generated by the "ALCHOLD REGISTER" and the corresponding DAC (IC24). When the two voltages equals, the ramp is stopped and switch IC44-10,11 is closed. The ALC voltage is now constant generated by the "ALCHOLD REGISTER" and thereby the gain of the Transmitter Signal Path is independent of the modulating signal.

When MEDIUM POWER is selected, the ALC voltage generated by the "ALCHOLD REGISTER" is increased by 0.93 V. In LOW POWER a 14 dB attenuator placed on the POWER AMPLIFIER ASSEMBLY 626 controlled by PAATT is activated and the ALC voltage is equal to the Full Power preset value.

6.5.2 Protection Circuits

6.5.2.1 Power Amplifier Protection

The Power Amplifier Protection can be divided into two main groups, SWR protection and thermal protection.

The SWR protection contains a reflected power and output voltage detector placed at the output of the POWER AMPLIFIER ASSEMBLY 626 . The output of the detector (PAPEAK) is connected to the TRANSCEIVER CONTROL BOARD 624 , PL2-7 and is OR'ed together with the FILPEAK voltage from the P.A. FILTER ASSEMBLY 627 628 or 629 . Now, if the SWR at the output of the POWER AMPLIFIER ASSEMBLY 626 increases during a transmission an error voltage is generated at IC42-1 exceeding the voltage generated by the "ALCHOLD REGISTER" thereby increasing the ALC voltage and reducing the output power within 1 ms to a permissible level.

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The output of the reflected power and output voltage detector is also used to make an independent local protection of the Power Amplifier by activating the 14 dB attenuator if the detector voltage exceeds 10 V. This ensures fully protection of the Power Amplifier if the ALC-loop should be faulty or disconnected. To reset the attenuator it is necessary to turn off the main power of the TRANSCEIVER in a few seconds.

The thermal protection consists of two thermoswitches mounted on the heatsink of the POWER AMPLIFIER ASSEMBLY and an averag-e/peak power detector.

One thermoswitch is activated if the heatsink temperature exceeds 100 deg. C. Thereby logical signal TC1 fed to the TRANSCEIVER CONTROL BOARD [624], PL2-5 goes low and the output power is reduced by 5 dB. This is carried out by changing the reference voltage from the "SETPOINT REGISTER" to 4.36 V and increasing the voltage from the "ALCHOLD REGISTER" by 0.82 V relative to the Full Power preset value.

The other thermoswitch is activated if the temperature of the heatsink exceeds 110 deg. C. In this case the supply voltage to the preamplifier is cut off.

The average power and the peak power are compared in IC41-3,2. If, in a Full Power transmission, the average power exceeds the peak power minus 3 dB, the logical signal at IC41-1 goes high. If this condition has been present during one minute, e.g. by transmitting CW with continuous key-down or broadcast mode telex, the output power will be reduced by 3 dB (SETPOINT voltage 5.71 V, ALCHOLD voltage increased by 0.54 V relative to Full Power preset value). The power will recover to Full Power level when the transmitter has been muted during two minutes.

To enable Full Power ARQ Telex Transmission the system accepts keying duty-cycles less than 50 % and modulation rates greater than 3 baud without power reduction.

6.5.2.2 ATU Protection

To protect the ANTENNA TUNING UNIT against excess current, for instance if the antenna is shortcircuited , an average current detector is provided. The output of the detector IANTAVR is connected to the TRANSCEIVER CONTROL BOARD [624], PL4-14 and is OR'ed together with the FILPEAK voltage from the P.A. FILTER ASSEMBLY [627] [628] or [629] . Now, if the average current exceeds 6 A during a transmission an error voltage is generated at IC42-1 exceeding the voltage generated by the "ALCHOLD REGIS-TER" thereby increasing the ALC voltage and reducing the out-put power and thereby the average current.

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If the SWR at the input of the ANTENNA TUNING UNIT exceeds 1:3 logical signal $\overline{\text{SWROK}}$ goes high and Power Display Annunciator on CONTROL UNIT front panel starts flashing informing the operator that a better antenna match might be obtained by carrying out a new Tune Sequence.

To prevent overheating of the ANTENNA TUNING UNIT a temperature sensor is incorporated. If the internal temperature of the ANTENNA TUNING UNIT exceeds 85 deg. C, logical signal TCO goes low and the output power is reduced by 5 dB. (SETPOINT voltage 4.36 V, ALCHOLD voltage increased by 0.82 V relative to Full Power preset value).

6.5.2.3 Reduced Power-Indication

In case of 5 dB reduced power condition due to thermal protection the annunciator "Reduced Power" on the CONTROL UNIT front panel is lit.

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APPENDIX TO CHAPTER 6

6.3.5 50 OHM ATU RELAY [644]

The ATU RELAY is a fast switching simplex relay (< 5 msec) which in combination with [630] requires only one coax cable to be connected between the TU and the ATU. The RELAY board is mounted inside the ATU and is controlled by PCB 640 .